CLAIM 12 AS IT SHOULD NOW READ:

12. A semiconductor device including a memory cell region and a peripheral circuit region, comprising:

a semiconductor substrate having a major surface;

an insulating film, having an upper surface, being formed on said major surface of said semiconductor substrate to extend from said memory cell region to said peripheral circuit region;

a capacitor lower electrode, including first and second lower electrodes being adjacent to each other through a part of said insulating film, being formed on said major surface of said semiconductor substrate to extend up to a vertical position substantially identical to that of said upper surface of said insulating film in said memory cell region; and

a capacitor upper electrode being formed on said capacitor lower electrode through a dielectric film to extend onto said upper surface of said insulating film,

said capacitor lower electrode including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface.